PTO 06-4503

CY=JA DATE=19931215 KIND=B2
PN=05-087027

READ WRITE METHOD FOR SEMICONDUCTOR DEVICE
[Handotai sochi ni okeru kakikomi, yomidashi hoho]

Hiroshi Ikeda, et al.

UNITED STATES PATENT AND TRADEMARK OFFICE
Washington, D.C. May 2006

Translated by: FLS, Inc.

PUBLICATION COUNTRY	(19):	JP
DOCUMENT NUMBER	(11):	5-87027
DOCUMENT KIND	(12): (13):	B2
PUBLICATION DATE	(43):	19870114
PUBLICATION DATE	(44):	19931214
APPLICATION NUMBER	(21):	60-144574
APPLICATION DATE	(22):	19850703
ADDITION TO	(61):	
INTERNATIONAL CLASSIFICATION	(51):	H01L 27/108
DOMESTIC CLASSIFICATION	(52):	
PRIORITY COUNTRY	(33):	
PRIORITY DATE	(32):	
PRIORITY NUMBER	(31):	

INVENTORS	(72):	IKEDA, HIROSHI; KATO, KOICHI
APPLICANT	(71):	AGENCY OF IND SCIENCE & TECH

TITLE	(54):	READ WRITE METHOD FOR SEMICONDUCTOR DEVICE
FOREIGN TITLE	[54A]:	HANDOTAI SOCHI NI OKERU KAKIKOMI, YOMIDASHI HOHO

(57) Claims

(1) A read write method for a semiconductor device, wherein a MOS transistor comprises a source-drain formed consisting of reverse-conductive impurities on both ends of an electrically floating conductive semiconductor layer and a gate electrode formed on the semiconductor layer via an insulating film, wherein during writing voltage not causing impact ionization is applied to the drain, the gate voltage is rapidly reduced from above the threshold to zero, wherein during deleting voltage causing impact ionization is applied to the drain and the gate voltage is rapidly reduced from above the threshold to zero, and wherein during reading voltage not causing impact ionization is applied to the drain, voltage above the threshold is applied to the gate and then voltage below the threshold is applied.

Detailed Description of the Invention

(Industrial Field of Application)

The present invention relates to a semiconductor memory device and, more specifically, to a read write method for a semiconductor device using a MOS transistor formed in a semiconductor layer on an insulator.

(Prior Art and Problem to be Solved)

Many different types of rewritable semiconductor memory have been developed, including floating gate avalanche injection MOS (FAMOS), stacked gate avalanche injection MOS (SAMOS), and metal nitride oxide semiconductors (MNOS).

Unfortunately, these semiconductor memory elements have the following problems. They have a structure in which the gate electrode is sealed in an insulating film, the insulating film below the gate electrode has a multilayer configuration, and the device requires a double electrode configuration. As a result, the configuration is complicated and the operation is very cumbersome compared to a normal MOSFET. A high gate voltage is required during the data writing operation, a circuit is required for this, and a high-voltage resistant transistor has to be used. This increases manufacturing costs.

(Purpose of the Invention)

In light of this situation, the purpose of the present invention is to provide a read write method for rewritable semiconductor devices with a simple configuration using a MOS transistor formed on top of an insulator.

(Summary of the Invention)

The framework of the present invention realizes a single memory element consisting of a single MOS transistor. By dynamically controlling the size of the voltage applied to the gate and drain of a MOS transistor formed on top of an insulator, the MOS transistor itself can perform memory functions.

The present invention is a read write method for a semiconductor device, wherein a MOS transistor comprises a source-drain formed consisting of reverse-conductive impurities on both ends of an electrically floating conductive semiconductor layer and a gate

electrode formed on the semiconductor layer via an insulating film, wherein during writing voltage not causing impact ionization is applied to the drain, the gate voltage is rapidly reduced from above the threshold to zero, wherein during deleting voltage causing impact ionization is applied to the drain and the gate voltage is rapidly reduced from above the threshold to zero, and wherein during reading voltage not causing impact ionization is applied to the drain, voltage above the threshold is applied to the gate and then voltage below the threshold is applied.

(Effect of the Invention)

The present invention realizes a memory element consisting of a single MOS transistor. As a result, it has a simple configuration and is easier than the prior art to manufacture. Because high voltage is not required, a circuit and element solution is [not] required. This lowers manufacturing costs.

(Working Examples of the Invention)

The following is a detailed explanation of the invention with reference to the working example in the drawings.

FIG 1 is a simplified diagram of the semiconductor device in a working example of the present invention. Here, a P-type silicon layer [21] (floating substrate) formed on top of an insulator [10] is doped with N-type impurities to form source and drain regions [22, 23]. A gate electrode [25] is formed via a gate oxide film [24] to complete a channel-length 1.2 μm N-type MOS transistor [20]. The silicon film [21] is created by depositing a polycrystalline or

amorphous silicon film such as an SiO_2 film on an insulator [10] and then beam annealing the silicon film to monocrystallize it. The silicon layer [21] floats.

The source [22] in the MOS transistor [20] is grounded, and the drain [23] and source [25] are connected to the sense circuit [30]. Because the sense circuit [30] reads and writes the data stored in the MOS transistor [20], the size of the voltage applied to the gate and drain is dynamically controlled.

In the sense circuit [30], voltage is generated during the writing and deleting of data in the following way. During the writing of data, as shown in FIG 2 (a), voltage that does not cause impact ionization is applied to the drain [23] and voltage above the threshold is applied to the gate [25]. The gate voltage is then suddenly lowered to zero. During the deleting of data, as shown in FIG 2 (b), voltage that causes impact ionization is applied to the drain [23], and the gate voltage is then suddenly lowered to zero. During the reading of data, gate voltage above the threshold is applied while voltage that does not cause impact ionization is being applied to the drain [23].

As in a conventional semiconductor memory element, the MOS transistor [20] is arranged on a matrix, and the gate and drain are connected by a word line and bit line to function as a memory circuit.

The following is an explanation of the operation of a device with this configuration.

First, if writing data, the source [22] is grounded, low positive voltage (e.g., 0.5 V) that does not cause impact ionization is applied to the drain [23], positive voltage above the threshold (e.g., 5 V) is then applied to the gate electrode [25], a channel is created below the insulating film [24] in the floating substrate [21], and the gate voltage is abruptly lowered below the gate electrode. When the gate voltage is lowered abruptly below the gate electrode, the electrons inside the channel are absorbed by the source-drain, a capacity bond is created between the channel and substrate, and the electric potential of the floating substrate [21] is lowered. The electrons supplied from the source-drain, and the holes inside the floating substrate [21] cause thermal annihilation, the hole concentration inside the floating substrate [21] becomes thinner, and the floating substrate [21] remains sharply biased to the negative with respect to the source [22]. When a negative bias is applied while back bias is being applied to the MOS transistor [20] in this state, tbe threshold voltage rises. When the drain current is measured and the floating substrate [21] has the same potential as the source [22], low current flows compared to when no data is stored in the semiconductor memory element (MOS transistor [20]).

When the data stored in the semiconductor memory element is deleted, it is exposed to light and electrons-holes are created inside the floating susbtrate [21]. Voltage that either returns the number of holes in the floating substrate [21] to the original number or causes impact ionization in the drain [23] (e.g., 5 V) is applied.

When the gate voltage is then applied and lowered suddenly below the threshold, many holes from the impact ionization remain in the floating substrate [21].

When the data stored in the semiconductor memory element is read, the drain [23] is connected to the bit line, and the bit line is charged with a predetermined voltage (e.g., 2.5 V). When the gate voltage [25] is raised above the threshold voltage, the drain current flows. Because the bit line voltage at this time is charged to a potential that does not cause impact ionization, when the voltage to the gate electrode [25] is lowered below the threshold to terminate the data reading operation, the floating substrate [21] remains biased to the negative and the data is preserved. If the floating substrate [21] is not biased when the potential of the gate electrode [25] is raised, electrons flow inside the floating substrate [25], the holes are forced downward, the floating substrate potential is raised, the threshold voltage is lowered, and a large drain current flows. At this time, the bit line is sensed and the potential causes impact ionization. When the potential of the gate electrode [25] is lowered again below the threshold to end the data reading operation, a large amount of holes remains in the floating substrate [21] and the data is stored.

In this working example, the MOS transistor [20] functioned as a memory element. In other words, a memory cell was created from a single MOS transistor [20]. Compared to memory cells of the prior art consisting of a single transistor and single capacitor, this memory

cell allows for greater integration and faster processing speeds. Because the element structure is simple, it is easy to manufacture.

The present invention is by no means restricted to this working example. For example, the MOS transistor does not have to be an N-type transistor. It can be a P-type transistor as well. Also the silicon layer does not have to be formed on an amorphous insulator (SOI) such as SiO_2. For example, it can be a layer (SOS) formed on a sapphire monocrystalline insulator. In addition, the bias conditions for applying voltage to the gate and drain of the MOS transistor can be adjusted depending on the physical properties of the MOS transistor being used. In other words, other variations are possible within the scope of the present invention.

Brief Explanation of the Drawings

FIG 1 is a simplified diagram of the semiconductor device in a working example of the present invention. FIG 2 a, b are signal diagrams used to explain the operation of the sense circuit used in the same device.

10 ... insulator, 20 ... N-type MOS transistor, 21 ... P-type silicon layer (floating substrate), 22 ... source, 23 ... drain, 24 ... gate oxide film, 25 ... gate electrode, 30 ... sense circuit

FIG 2

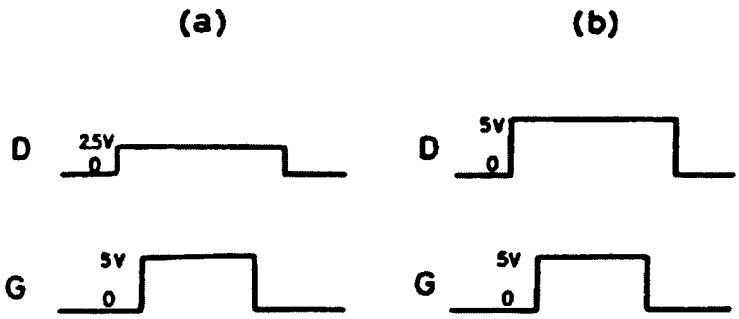
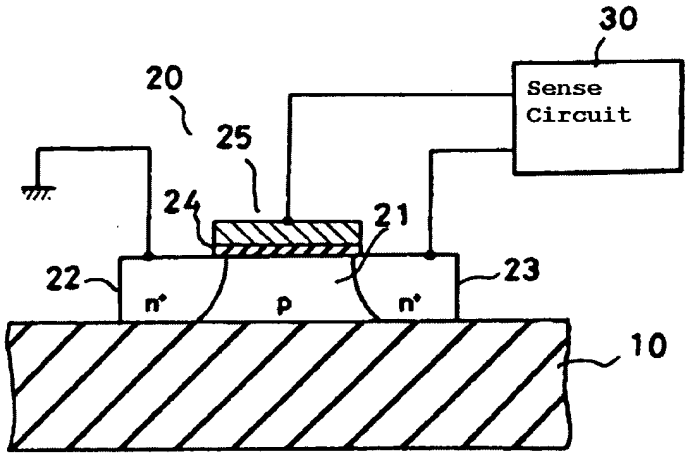

(a)
(b)
D
25V
0
G
5V
0
D
5V
0
G
5V
0

FIG 1


30
Sense
Circuit
20
25
24
21
22
23
n+
p
n+
10